Introduction

Xillyp2p is a straightforward, intuitive and efficient end-to-end solution for point-to-point data transport between two FPGAs connected through a Multi-Gigabit Transceiver (MGT) or other types of serial or parallel I/O.

The FPGA designer interacts with the Xillyp2p IP core through standard FIFOs: On one FPGA, data is written to a FIFO, and on the other FPGA, this data is read from a FIFO. The IP core creates an illusion of one FIFO spanning across both FPGAs, having data write ports on one FPGA, and data read ports on the other. The data transport is reliable; all data is delivered error-free on the receiving side, regardless of possible bit errors on the underlying physical link. As with any FIFO, even a single word in the FIFO becomes visible on the other side, and yet the IP core utilizes the physical link's bandwidth efficiently for larger amounts of data.

Hotplugging the physical link is seamlessly supported.

An online tool (the IP Core Factory) is available on the website for immediate configuration and download of custom Xillyp2p IP cores per specification: The number of streams, their direction, their data width, expected bandwidth and other parameters.

IP core facts	
Supported FPGAs	**AMD / Xilinx**: All Series-7, all Ultrascale and Ultrascale+, Versal ACAP, Zynq-7000 / Zynq Ultrascale+ The FPGAs on each side may belong to different FPGA families.
Transport	MGT or general-purpose I/O with or without SERDES
Bandwidth	From 10 Mbit/s to the physical link's available data rate
Deliverables	• Pair of IP cores in netlist format (EDIF) • Instantiation templates
Applications	FPGA interconnect on the same PCB or through a backplane, data acquisition / playback with a remotely located FPGA, long-distance data transport or electrical isolation using optical fiber, data link with peripheral equipment through a cable (cameras, displays, sensors, radio transceivers etc.), cost reduction of I/O-intensive applications by splitting the project into several FPGAs.

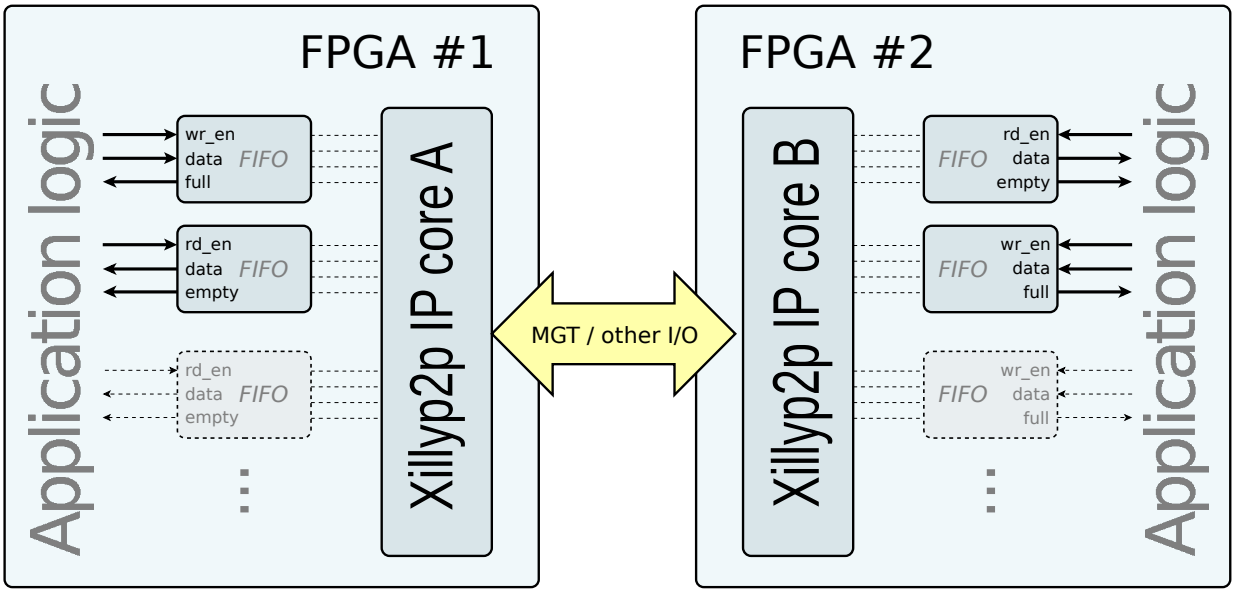

Figure 1: Simplified block diagram of two FPGAs using Xillyp2p

Physical link

In the common usage scenario, the IP cores on both sides use the FPGA's MGT resource to communicate with each other. The MGT is only used to serialize and deserialize data for transmission and reception. All other functionalities required for a serial data link (e.g. word alignment, synchronization, scrambling, frequency difference compensation, high-level protocol, error detection and retransmission) are implemented in the IP core.

The IP core interfaces with its physical link by sending and/or receiving bit vectors of raw data. The IP core is primarily intended for MGT-based physical links; however any physical link that is represented as a bit vector for transmission and reception can be used with Xillyp2p. This includes an arbitrary number of physical wires connected between the two FPGAs (possibly a single wire). It's also possible to use the I/O block's SERDES feature for the purpose of serializing and deserializing the bit vector. When regular FPGA I/O is used, it's the application logic's responsibility to ensure that the receiving side samples its inputs with proper timing (an MGT has this feature built-in).

The physical link can be bidirectional or unidirectional.

Flow control

Each application data stream has an optional flow control feature. This is implemented by connecting the FIFO's "full" output port to the IP core on the receiving side. When this feature is used, the IP core respects the "full" signal and avoids writing to the FIFO when it is full. The IP core implements an efficient flow control mechanism that holds back the data flow on the specific application data stream as necessary.

From the application user's perspective, this flow control mechanism is another aspect of the illusion of a FIFO that spans across the two FPGAs.

Flow control is available only with a bidirectional physical link.

Bit error handling

The IP core performs CRC32 verification to ensure that all data delivered to the receiving application logic is error-free. When the physical link is bidirectional, a retransmission mechanism provides transparent correction of bit errors occurring on the physical link. A bit error rate (BER) below 10^{-6} is recommended, as a performance hit may otherwise occur.

In a unidirectional link setting, the receiving IP core has no way to request a retransmission. Accordingly, a bit error on the physical link causes all application data streams to halt before the point the error was detected, ensuring all delivered data is error-free. Resumption to normal operation is requested by the application logic by virtue of dedicated input ports.

Optional End-of-Packet feature

Even though the FIFO illusion presented by the IP core is naturally inclined towards a continuous stream of data, it is possible to easily transmit the data as packets by using the End-of-Packet port assigned to each application data stream. When this port is asserted on the transmitting side along with a data word, this word is marked as the last in a packet. As a result, the End-of-Packet output port on the receiving side is asserted along with the same data word. The End-of-Packet feature has no significant impact on performance nor latency, and is intended only for organizing the data to better suit the application.

Support

Intensive, focused, and comprehensive support guarantees rapid integration of the Xillyp2p IP core with application logic.

Licensing

The Xillyp2p core has several license variants:

- No-fee evaluation license: A fully functional core, possibly tailored to the customer's specification, for unlimited evaluation in the real project environment, running on real data under real conditions.
- Production license: Royalty-free Xilinx SignOnce license (or similar) for an unlimited number of copies.
- No-fee educational license: Unlimited use for undergraduate student projects, pure academic research and similar projects.

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