Introduction

Xillybus is a straightforward, intuitive, efficient DMA-based end-to-end turnkey solution for data transport between an FPGA and a host running Linux or Microsoft Windows.

The FPGA designer as well as the host application programmer interact with Xillybus through well-known interfaces: The FPGA application logic connects to the IP core through standard FIFOs; the user application on the host performs plain file I/O operations on pipe-like device files. Streaming data moves naturally between the FIFO and the file handler opened by the host application. There is no specific API involved.

An online tool (the IP Core Factory) is available on the website for immediate configuration and download of custom-tailored Xillybus IP cores per specification: The number of streams, their direction, their data width, bandwidth expectations and other parameters.

IP core facts	
Supported FPGAs	**Xilinx**: Virtex-5T, Spartan-6T, Virtex-6T, all Series-7, all Ultrascale and Ultrascale+, Zynq-7000 / Ultrascale+ **Altera**: Cyclone, Stratix, Arria and HardCopy, having Hard IP for PCI Express + Cyclone V SoC
Transport	PCI Express, AXI3 and AXI4
Bandwidth	Up to 3.5 GB/s simultaneously in both directions, depending on FPGA and host capabilities
Operating systems	Linux > 2.6.36 (possibly older) Microsoft Windows 7, 8 and 10 (32 or 64 bit)
Deliverables	• IP core in netlist format (NGC/EDIF/QXP) • Driver for Linux (source code) or Windows (digitally signed binary) • Sample user space applications (source code)
Applications	Data acquisition and playback, interface with hardware, custom computer peripherals, in-hardware logic verification, coprocessing and more.
Logic consumption	110 LUTs/stream + 2500 LUTs (estimated for Xilinx) + a small number of RAMs

FPGA design interface

Figure 1 depicts a simplified block diagram showing the connection of one data stream in each direction (in a typical application there are several). The Xillybus IP core communicates data with the user logic through a standard FIFO ("Application FIFO" in the diagram), which is supplied by the IP core's user. This gives the FPGA designer the freedom to decide the FIFO's depth and its interface with the application logic.

This setting relieves the FPGA designer completely from managing the data traffic with the host. Rather, the Xillybus core checks the FIFOs "empty" or "full" signals (depending on data direction), and initiates data transfers when the FIFO is ready for it.

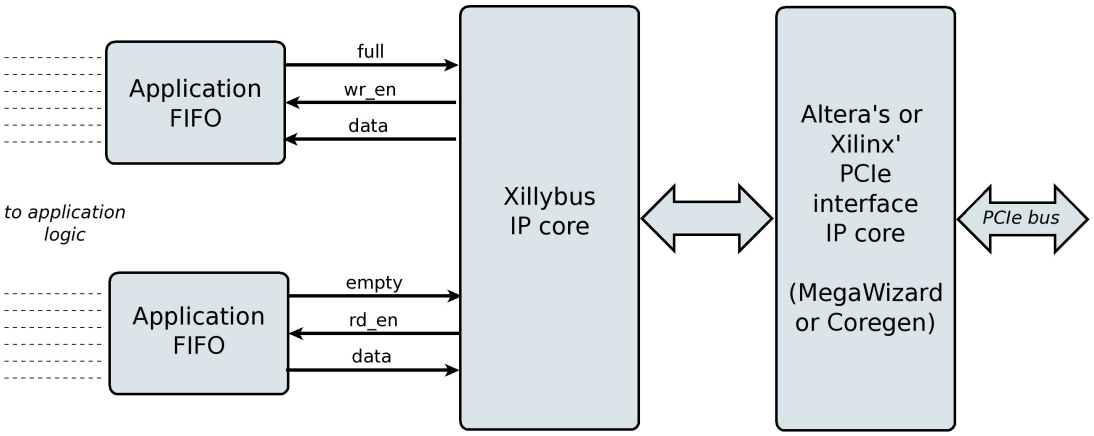

Figure 1: Simplified FPGA block diagram of Xillybus using PCIe transport (AXI3/4 also available)

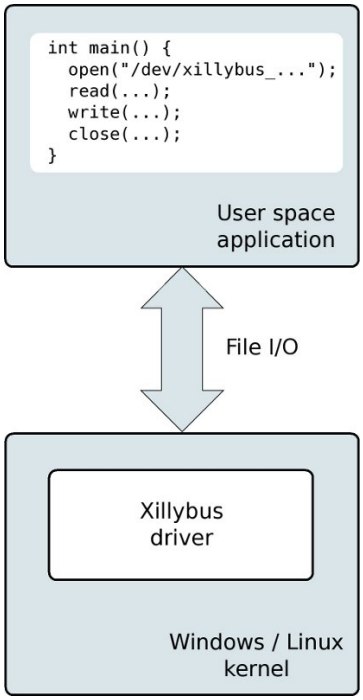

Figure 2: Host interface block diagram

Host application interface

There is no kernel-space or hardware-related programming necessary on the host side, nor any need to link with a particular software library. Any practical programming language can be used to access Xillybus streams without a specific extension.

The host driver generates device files that behave like named pipes: They are opened, read from and written to just like any file, but behave much like pipes between processes or TCP/IP streams. And like the TCP/IP socket, the Xillybus stream is designed to work well with high-rate data transfers as well as single bytes arriving or sent occasionally.

One driver binary version supports any Xillybus IP core configuration: The streams and their attributes are auto-detected by the driver when it's loaded into the host's operating system, and device files are created accordingly. In Windows machines, these device files are accessed as \\.\xillybus_something. On Linux, they appear as /dev/xillybus_something. The specific names are chosen by customer.

Support

Intensive, focused, and comprehensive lifetime support guarantees a rapid integration of the Xillybus IP core, application logic and software.

Licensing

The Xillybus core has several license variants:

- No-fee evaluation license: A fully functional core, possibly tailored per customer's spec, for unlimited evaluation in the real project environment, running on real data under real conditions.
- Production license: Royalty-free Xilinx SignOnce license (or similar) for an unlimited number of copies.
- Single-copy license: A lower-cost Xilinx SignOnce license (or similar) limited to one single physical FPGA device at any given moment.
- No-fee educational license: Unlimited use for undergraduate student projects, pure academic research etc.

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